CLAIMS

1. A switching circuit having a first field effect transistor (35) and a second field effect transistor (36) connected in series between an input terminal (37) and a ground terminal (38), wherein a source (43) of the first transistor (35) is connected to the drain (44) of the second transistor (36) and a source (40) of the second transistor (36) is connected to the ground terminal (38), the circuit comprising:

control means (52, 58; 53, 59) for driving the first and second transistors (35, 36) alternately such that there is a dead time period during which both transistors are off; and

means (83, 84) for adjusting the length of the dead time period according to a voltage difference between the drain (39, 44) and the source (43, 40) of the first or second transistor.

2. A switching circuit according to claim 1, wherein the first and/or the second transistors (35, 36) are constructed on an integrated circuit die, each of said transistors (35, 36) having respective drain (39, 44) and source (43, 40) regions on said die, further comprising sensing means (81, 82) for sensing the voltage difference between the drain (39, 44) and the source (43, 40) of the first or second transistors (35, 36), wherein the sensing means has a first connection (72, 68) which is directly connected to the source region (43, 40) of the first or second transistor (35, 36).

3. A switching circuit according to claim 2, wherein the sensing means (81, 82) has a second connection (71, 67) which is directly connected to the drain region (39, 44) of the first or second transistor (35, 36).

4. A switching circuit according to claim 2 or 3, wherein the first and/or second connections (72, 68, 71, 67) are Kelvin connections.

5. A switching circuit according any one of claims 2 to 4, wherein the sensing means (81, 82) senses the voltage difference during the dead time period.

6. A switching circuit according to any preceding claim, wherein the adjusting means (83, 84) adjusts the length of future dead time periods according to the voltage difference during the dead time period.

7. A switching circuit according to any preceding claim, wherein the adjusting means (83, 84) adjusts the length of the dead time period according to the length of time that the voltage difference exceeds a threshold voltage.

8. A switching circuit according to any preceding claim, wherein the adjusting means (83, 84) adjusts the length of the dead time period according to the magnitude by which the voltage difference exceeds a threshold voltage.

9. A switching circuit according to any preceding claim, wherein the adjusting means (83, 84) adjusts the length of the dead time period such that the length of the dead time period is exponentially dependent on the magnitude by which the voltage difference exceeds the threshold voltage.

10. A switching circuit according to any preceding claim, wherein the adjusting means (83, 84) adjusts the length of the dead time period such that the length of the dead time period is linearly dependent on the length of time for which the voltage difference exceeds a threshold value.

11. A switching circuit according to any preceding claim, comprising circuitry to prevent the first transistor (35) from turning on until the second transistor (36) has turned off.

12. A switching circuit according to any preceding claim, comprising circuitry to prevent the second transistor (36) from turning on until the first transistor (35) has turned off.

13. A dc-dc converter circuit comprising the switching circuit of any preceding claim.

14. A method of operating a switching circuit having a first field effect transistor (35) and a second field effect transistor (36) connected in series between an input terminal (37) and a ground terminal (38), wherein a source (43) of the first transistor (35) is connected to the drain (44) of the second transistor (36) and a source (40) of the second transistor (36) is connected to the ground terminal (38), the method comprising:

driving the first and second transistors (35, 36) alternately such that there is a dead time period during which both transistors (35, 36) are off; and

adjusting the length of the dead time period according to a voltage difference between the drain (44) and the source (40) of the first or second transistor (35, 36).

15. A switching circuit having a first field effect transistor (35) and a second field effect transistor (36) connected in series between an input terminal (37) and a ground terminal (38), wherein a source (40) of the first transistor (35) is connected to the drain (44) of the second transistor (36) and a source (40) of the second transistor (36) is connected to the ground terminal (38), the circuit comprising:

control means for driving said first and second transistors (35, 36) alternately such that there is a dead time period during which both transistors (35, 36) are off; and

means (83, 84) for adjusting the length of the dead time period according to a voltage difference between the drain (44) of the second transistor and the ground terminal (38), wherein

the adjusting means (83, 84) adjusts the length of the dead time period according to the length of time for which the voltage difference exceeds a threshold value.

16. A switching circuit according to claim 15, wherein the adjusting means (83, 84) adjusts length of the dead time period according to the magnitude by which the voltage difference exceeds the threshold voltage.

17. A switching circuit according to claim 15 or 16, wherein the adjusting means (83, 84) adjusts the length of the dead time period such that the length of the dead time period is exponentially dependent on the magnitude by which the voltage difference exceeds the threshold voltage.

18. A switching circuit according to claim 15, 16 or 17, wherein the adjusting means (83, 84) adjusts the length of the dead time period such that the length of the dead time period is linearly dependent on the length of time for which the voltage difference exceeds the threshold value.